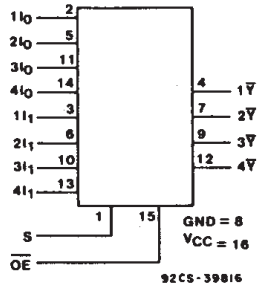


CD54/74HC258 CD54/74HCT258



Data sheet acquired from Harris Semiconductor
SCHS276

High-Speed CMOS Logic



FUNCTIONAL DIAGRAM

Quad 2-Input Multiplexer with 3-State Inverting Outputs

Type Features:

- Buffered inputs
- Typical CD54/74HC258 propagation delay = 7 ns
@ $V_{CC} = 5\text{ V}$, $C_L = 15\text{ pF}$, $T_A = 25^\circ\text{C}$

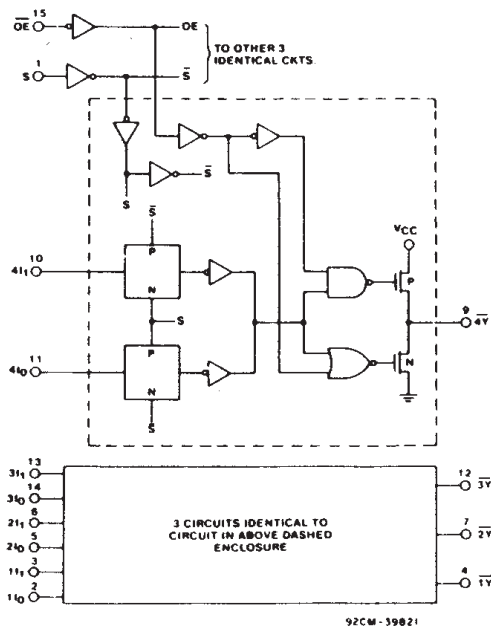
The RCA-CD54/74HC258 and CD54/74HCT258 are quad 2-input multiplexers which select four bits of data from two sources under the control of a common Select input (S). The Output Enable input (\overline{OE}) is active LOW. When \overline{OE} is HIGH, all of the outputs (1Y-4Y) are in the high impedance state regardless of all other input conditions.

Moving data from two groups of registers to four common output busses is a common use of the 258. The state of the Select input determines the particular register from which the data comes. It can also be used as a function generator.

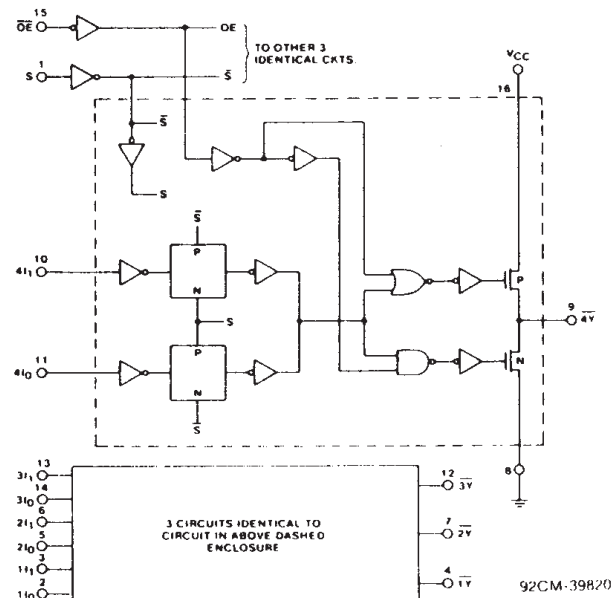
The CD54HC/HCT258 are supplied in 16-lead hermetic dual-in-line ceramic packages (F suffix). The CD74HC/HCT258 are supplied in 16-lead dual-in-line plastic packages (E suffix) and in 16-lead dual-in-line surface mount plastic packages (M suffix). Both types are also available in chip form (H suffix).

Family Features:

- Fanout (Over Temperature Range):
Standard Outputs - 10 LSTTL Loads
Bus Driver Outputs - 15 LSTTL Loads
- Wide Operating Temperature Range:
CD74HC/HCT/HCU: -40 to $+85^\circ\text{C}$
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LSTTL Logic ICs
- Alternate Source is Philips/Signetics
- CD54HC/CD74HC Types:
2 to 6 V Operation
High Noise Immunity:
 $N_{IL} = 30\%$, $N_{IH} = 30\%$ of V_{CC} ; @ $V_{CC} = 5\text{ V}$
- CD54HCT/CD74HCT Types:
4.5 to 5.5 V Operation
Direct LSTTL Input Logic Compatibility
 $V_{IL} = 0.8\text{ V Max.}$, $V_{IH} = 2\text{ V Min.}$
CMOS Input Compatibility
 $I_1 \leq 1\text{ }\mu\text{A}$ @ V_{OL} , V_{OH}



CD54/74HC258 Logic Diagram



CD54/74HCT258 Logic Diagram

CD54/74HC258 CD54/74HCT258

MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE, (V _{CC}):	-0.5 to + 7 V
(Voltages referenced to ground)	
DC INPUT DIODE CURRENT, I _{IK} (FOR V _i < -0.5 V OR V _i > V _{CC} + 0.5V)	±20mA
DC OUTPUT DIODE CURRENT, I _{OK} (FOR V _o < -0.5 V OR V _o > V _{CC} + 0.5V)	±20mA
DC DRAIN CURRENT, PER OUTPUT (I _o) (FOR -0.5 V < V _o < V _{CC} + 0.5V)	±35mA
DC V _{CC} OR GROUND CURRENT (I _{CC})	±70mA
POWER DISSIPATION PER PACKAGE (P _D):	500 mW
For T _A = -40 to +60°C (PACKAGE TYPE E)	Derate Linearly at 8 mW/°C to 300 mW
For T _A = +60 to +85°C (PACKAGE TYPE E)	Derate Linearly at 8 mW/°C to 300 mW
For T _A = -55 to +100°C (PACKAGE TYPE F, H)	Derate Linearly at 8 mW/°C to 300 mW
For T _A = +100 to +125°C (PACKAGE TYPE F, H)	Derate Linearly at 8 mW/°C to 300 mW
For T _A = -40 to +70°C (PACKAGE TYPE M)	Derate Linearly at 8 mW/°C to 300 mW
For T _A = +70 to +125°C (PACKAGE TYPE M)	Derate Linearly at 6 mW/°C to 70 mW
OPERATING-TEMPERATURE RANGE (T _A):	
PACKAGE TYPE F, H	-55 to +125°C
PACKAGE TYPE E, M	-40 to +85°C
STORAGE TEMPERATURE (T _{stg})	-65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max.	+265°C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm) with solder contacting lead tips only	+300°C

RECOMMENDED OPERATING CONDITIONS:

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

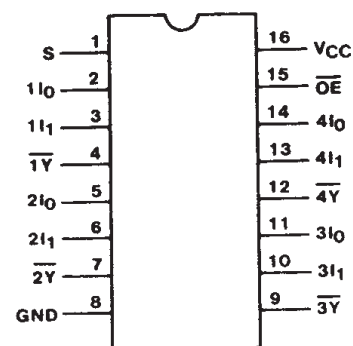
CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T _A = Full Package-Temperature Range) V _{CC} .*			V
CD54/74HC Types	2	6	
CD54/74HCT Types	4.5	5.5	
DC Input or Output Voltage V _i , V _o	0	V _{CC}	V
Operating Temperature T _A :			°C
CD74 Types	-40	+85	
CD54 Types	-55	+125	
Input Rise and Fall Times t _r , t _f			ns
at 2 V	0	1000	
at 4.5 V	0	500	
at 6 V	0	400	

*Unless otherwise specified, all voltages are referenced to Ground.

FUNCTION TABLE

Output Enable	Select Input	Data Inputs		Output
		I ₀	I ₁	
\overline{OE}	S	I ₀	I ₁	\overline{Y}
H	X	X	X	Z
L	L	L	X	H
L	L	H	X	L
L	H	X	L	H
L	H	X	H	L

H = High level voltage
L = Low level voltage
X = Don't care.
Z = High impedance (off) state



92CS-39015

TERMINAL ASSIGNMENT

CD54/74HC258 CD54/74HCT258

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CD74HC258/CD54HC258										CD74HCT258/CD54HCT258								UNITS																				
	TEST CONDITIONS			74HC/54HC TYPES			74HC TYPE		54HC TYPE			TEST CONDITIONS		74HCT/54HCT TYPES			74HCT TYPE			54HCT TYPE																			
	V _I V	I _O mA	V _{CC} V	+25°C			-40/ +85°C		-55/ +125°C			V _I V	V _{CC} V	+25°C			-40/ +85°C			-55/ +125°C																			
				Min	Typ	Max	Min	Max	Min	Max	Min			Max	Min	Max	Min	Max																					
High-Level Input Voltage V _{IH}			2	1.5	—	—	1.5	—	1.5	—	—	4.5		2	—	—	2	—	2	—	V																		
			4.5	3.15	—	—	3.15	—	3.15	—	—	to		—	—	—	—	—	—	—																			
			6	4.2	—	—	4.2	—	4.2	—	—	5.5		—	—	—	—	—	—	—																			
Low-Level Input Voltage V _{IL}			2	—	—	0.5	—	0.5	—	0.5	—	4.5		—	—	0.8	—	0.8	—	0.8	V																		
			4.5	—	—	1.35	—	1.35	—	1.35	—	to		—	—	—	—	—	—	—																			
			6	—	—	1.8	—	1.8	—	1.8	—	5.5		—	—	—	—	—	—	—																			
High-Level Output Voltage V _{OH}	V _{IL}	-0.02	2	1.9	—	—	1.9	—	1.9	—	V _{IL}	4.5	4.4	—	—	4.4	—	4.4	—	4.4	—	V																	
or			4.5	4.4	—	—	4.4	—	4.4	—	or																												
CMOS Loads	V _{IH}		6	5.9	—	—	5.9	—	5.9	—	V _{IH}																												
TTL Loads (Bus Driver)	V _{IL}	-6	4.5	3.98	—	—	3.84	—	3.7	—	V _{IL}	4.5	3.98	—	—	3.84	—	3.7	—	3.7	—	V																	
or			6	5.48	—	—	5.34	—	5.2	—	or																												
V _{IH}			7.8	6	—	—	0.26	—	0.33	—	0.4																												
Low-Level Output Voltage V _{OL}	V _{IL}	0.02	2	—	—	0.1	—	0.1	—	0.1	V _{IL}	4.5	—	—	0.1	—	0.1	—	0.1	—	0.1	V																	
or			4.5	—	—	0.1	—	0.1	—	0.1	or																												
CMOS Loads	V _{IH}		6	—	—	0.1	—	0.1	—	0.1	V _{IH}																												
TTL Loads (Bus Driver)	V _{IL}	6	4.5	—	—	0.26	—	0.33	—	0.4	V _{IL}	4.5	—	—	0.26	—	0.33	—	0.4	—	0.4	V																	
or			6	4.5	—	—	0.26	—	0.33	—	0.4																												
V _{IH}			7.8	6	—	—	0.26	—	0.33	—	0.4																												
Input Leakage Current I _I	V _{CC}	6	—	—	±0.1	—	±1	—	±1	—	Any Voltage Between V _{CC} & Grid	5.5	—	—	±0.1	—	±1	—	±1	—	±1	μA																	
or	Gnd																																						
Gnd																																							
Quiescent Device Current I _{CC}	V _{CC}	0	6	—	—	8	—	80	—	160	V _{CC}	5.5	—	—	8	—	80	—	160	—	160	μA																	
or	Gnd																																						
Gnd																																							
Additional Quiescent Device Current per input pin: 1 unit load ΔI _{CC} *											V _{CC} -2.1	4.5	—	100	360	—	450	—	490	—	490	μA																	
											5.5	to	—	—	—	—	—	—	—	—	—																		
3-State leakage current I _{OZ}	V _{IL}	V _O = V _{CC}	6	—	—	±0.5	—	±5	—	±10	V _{IL}	5.5	—	—	±0.5	—	±5	—	±10	—	±10	μA																	
or		or																										or											
V _{IH}		Gnd																										V _{IH}											

*For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

HCT Input Loading Table

Input	Unit Loads*
Data	0.5
S	1.5
OE	1.5

*Unit Load is ΔI_{CC} limit specified in Static Characteristic Chart, e.g., 360 μA max. @ 25°C.

CD54/74HC258 CD54/74HCT258

SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25°C, Input t_r, t_f = 6 ns)

CHARACTERISTIC	CL (pF)	TYPICAL		UNITS
		HC	HCT	
nI _O , nI _I , to \bar{Y} , t_{PHL} t_{PLH}	15	7	11	ns
\bar{OE} to \bar{Y}	t_{PZL} t_{PZH}	15	11	ns
	t_{PLZ} t_{PHZ}	15	12	ns
S to \bar{Y}	t_{PHL} t_{PLH}	15	14	ns
Power Dissipation Capacitance*	C _{PD}	—	49	pF

*C_{PD} is used to determine the dynamic power consumption, per multiplexer.
 $P_D = V_{CC}^2 f_i (C_{PD} + C_L)$ where: f_i = input frequency
 C_L = output load capacitance
 V_{CC} = supply voltage

SWITCHING CHARACTERISTICS (C_L = 50 pF, Input t_r, t_f = 6 ns)

CHARACTERISTIC	V _{CC}	25°C				-40°C to +85°C				-55°C to +125°C				UNITS	
		HC		HCT		74HC		74HCT		54HC		54HCT			
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
Propagation Delay, nI _O , nI _I , to \bar{Y} (Fig. 2)	t_{PLH}	2	—	95	—	—	—	120	—	—	—	145	—	—	ns
	t_{PHL}	4.5	—	19	—	27	—	24	—	34	—	29	—	41	
		6	—	15	—	—	—	20	—	—	—	25	—	—	
Propagation Delay S to \bar{Y} (Fig. 3)	t_{PLH}	2	—	140	—	—	—	175	—	—	—	210	—	—	ns
	t_{PHL}	4.5	—	28	—	34	—	35	—	43	—	42	—	51	
		6	—	24	—	—	—	30	—	—	—	36	—	—	
Propagation Delay \bar{OE} to Y (Fig. 4)	t_{PZL}	2	—	140	—	—	—	175	—	—	—	210	—	—	ns
	t_{PZH}	4.5	—	28	—	28	—	35	—	35	—	42	—	42	
		6	—	24	—	—	—	30	—	—	—	36	—	—	
Propagation Delay \bar{OE} to Y (Fig. 4)	t_{PLZ}	2	—	150	—	—	—	190	—	—	—	225	—	—	ns
	t_{PHZ}	4.5	—	30	—	30	—	38	—	38	—	45	—	45	
		6	—	26	—	—	—	33	—	—	—	38	—	—	
Output Transition Time (Fig. 2)	t_{TLH}	2	—	60	—	—	—	75	—	—	—	90	—	—	ns
	t_{THL}	4.5	—	12	—	12	—	15	—	15	—	18	—	18	
		6	—	10	—	—	—	13	—	—	—	15	—	—	
Input Capacitance	C _I		—	10	—	10	—	10	—	10	—	10	—	10	pF
3-State Output Capacitance	C _O		—	20	—	20	—	20	—	20	—	20	—	20	pF

CD54/74HC258 CD54/74HCT258

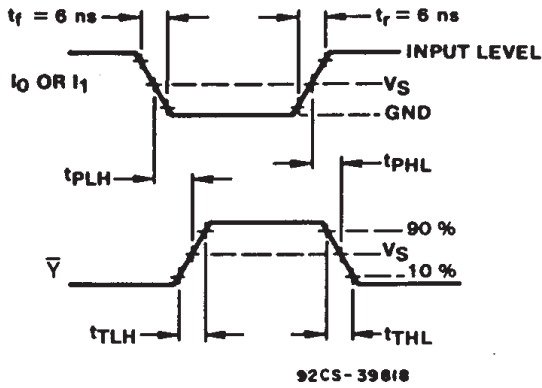


Fig. 2 - Select to output delays.

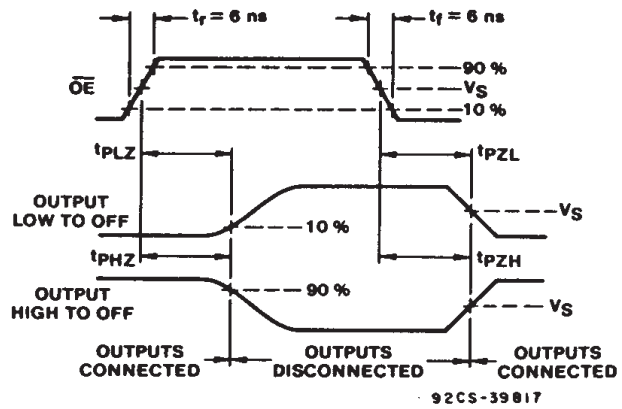


Fig. 4 - Output Enable to output propagation delays.

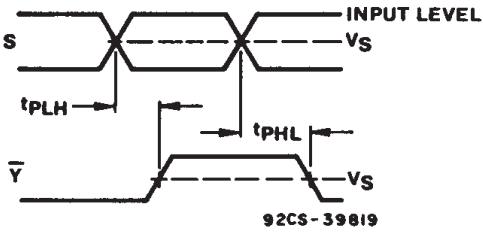


Fig. 3 - Select to output propagation delays.

	54/74HC	54/74HCT
Input Level	V_{CC}	3V
Switching Voltage, V_S	50% V_{CC}	1.3 V